US-PAT-NO: 4841522

DOCUMENT-IDENTIFIER: US 4841522 A

TITLE: Time division channel switching circuit

---------- KWIC ---------

Detailed Description Text - DETX (6):

A conventional switching circuit for such sub **channel** switching is known such as shown in FIG. 4A. In FIG. 4A, reference numeral 21 designates a **channel** memory, which has a capacity of nm sub **channels** corresponding to one frame (T sec), 22 and 23 input and output secondary highways, 24 a multiplexing circuit, 25 a distribution circuit, 26 and 27 input and output highways, 28 a counter which counts from 1 to nm with a clock timing of T/nm within the frame period T, and 29 a control memory which has a capacity of nm words for storing addresses of the **channel** memory 21. The operation of this switching circuit will herein below be described with reference to FIG. 4A and FIG. 4B which shows the read/write cycle for the **channel** memory 21. The counter 28 is **synchronized** with the frame period of the input secondary highway 22. That is, while information of a k sub **channel** in an i **channel** is being transmitted over the input secondary highway 22, the contents of the counter 28 are of m(i-1)+k. By sequential **writing** of the information on the input secondary highway 22 into the **channel** memory 21 through use of the **count** value as the **address** therefor, the whole **channel**/sub **channel** information will have been **written into the channel** memory 21 at the end of the period T. On the other hand, the control memory 29 has prestored therein **addresses** for randomly **reading** out information from the **channel** memory 21. For instance, let it be assumed that a value of m(i-1)+k is stored in the control memory 29 at an address (m(j-1)+l corresonding to an l sub **channel** in a j **channel** on the output secondary highway 23. In this instance, when the counting value of the counter 28 has reached a value of (m(j-1)+l, the contents [(m(i-1)+k] at the address m(j-1)+l of the control memory 29 are read out using the above counting value as the address therefor, and the contents of the **channel** memory 21 are read out using the read-out contents m(i-1)+k as the address therefor, by which the information of the k sub **channel** in the i **channel** on the input secondary highway 22 can be switched to the l sub **channel** in the j **channel** on the output secondary highway 23.

US-PAT-NO: 5353281

DOCUMENT-IDENTIFIER: US 5353281 A

TITLE: Intermittenceless switching system

---------- KWIC ---------

Brief Summary Text - BSTX (14):

The **read-address** change switch 18 is actuated by an **address** indicated by an output of the **counter** 16 in **synchronization with the write-address** change switch 15 as described previously. Numbers 1, 2, . . . n designated on the connection control memory 14 represent read addresses of the speech path memory 13 for each time **slot,** n is equal to 4, n=4, because of the 4**-channels** as shown in FIG. 9A, which was previously described as the speech path memory 13 Thus, each address of the connection control memory 14 and the contents stored in each address thereof indicate which time **slot** on the incoming highway 11 is transferred to which time **slot** on the outgoing highway 12, thereby representing the connection state of the speech path on the time division switch 6. A microprocessor 19 rewrites the contents of the connection control memory 14 through a data bus 20 and an address bus 21 in response to a call from a switching system, as required, to switch the connection state of the speech path of the time division switch 6.

Detailed Description Text - DETX (3):

The first difference from FIG. 8 is that the time division switch 6 has a speech path memory 13, a write-address change switch 15 and a read-address change switch 17, which are exactly identical components shown in FIG. 1, also having a speech path memory 23, a write-address change switch 25 and a read-address change switch 27. These pairs of the speech path memories 13 and 23, the write-address change switches 15 and 25, and the read-address change switches 17 and 27 are connected with an incoming highway 11 and an outgoing highway 12, respectively, through frame change switches 43 and 44 which are switched at a frame-timing. Also, the frame change switches 43 and 44 are switched by an output signal 41 of a most significant bit M of a counter 16 which counts timing of time **slots**. The most significant bit M alternately changes "1" and "0" at every frame, and is a type of adding one more bit to the most significant bit M of the counter 16 shown in FIG. 8. In the frame change

switches 43 and 44 shown in FIG. 1, in case of a frame which is connected with the writing side of the speech path memory 23 to the incoming highway 11, the outgoing highway 12 is connected with the reading side of the speech path memory 13, and in case of a frame which is connected with the speech path memory 13 to the incoming highway 11, the outgoing highway 12 is connected with the speech path memory 23, so that above connection operation is alternately carried out at every frame. The **write-address** change switches 15 and 25 and the **read-address** change switches 17 and 27 are actuated by **reading** results from an output C of the **counter** 18 and the connection control memory 14, respectively, thereby to be indicated its **address in synchronization** with each other. As a result, information of all time **slots** of a frame is written into either one of the speech path memories 13 or 23, in the following frame, the information is, in turn, read from one of the speech path memory 13 or 23 in the order of addresses indicated by the connection control memory 14. The switching operation above is illustrated in FIGS. 2A, 2B, 2C and 2D so that the state of the time **slot** T2 on the incoming highway 11 connecting with the time **slot** T3 on the outgoing highway 12 through the time division switch 6, is switched to the state thereof on the incoming highway 11 connecting with the time **slot** T1 on the outgoing highway 12.

US-PAT-NO: 4206322

DOCUMENT-IDENTIFIER: US 4206322 A

TITLE: Time-division switching system for multirate data

---------- KWIC ---------

Detailed Description Text - DETX (23):

All data words on time-multiplex line 101 are sequentially placed in a data register 508. A **synchronization** circuit 501 is also connected to the incoming time-multiplex line 101 and derives timing signals to control the data word distribution from the signals on that time-multiplex line. **Synchronization** circuit 501 generates a recurring sequence of pulses, one being associated with each incoming **channel** on time-multiplex line 101. These pulses are transmitted to a **channel counter** 502, which generates digital signals representing the recurring numerical sequence 0 through 127. After **channel** 127 is **counted,** **channel counter** 502 is reset to zero and the **count** begins again. The output of **channel counter** 502 is transmitted to an **address** register 507 associated with all of the twenty memories of input buffer memory 105 and to a decoder circuit 503. Decoder circuit 503 is a 1 out of 128 decoder which responds to each **channel** designation from **channel counter** 502 by enabling a predefined 1 of 128 subrate **counters** of which subrate **counter** 504, associated with **channel** O, and subrate **counter** 505, associated with **channel** 127, are shown. Each subrate **counter** includes a register circuit and a **counter** which generate a recurring sequence from zero through s where s is the maximum number of subscribers sharing the incoming **channel** associated with that subrate **counter**. For example, if the subrate **counter** 504 were associated with 2.4 kilobit customers, its internal **counter** would generate the sequence zero through twenty every twenty frames. The output of the subrate **counter** selected by decoder circuit 503 is transmitted to a memory enable circuit 506. Memory enable circuit 506 is a 1 out of 20 decoder which responds to the **count** transmitted to it from the selected subrate **counter** by enabling one of the twenty buffer memories making up input buffer memory 105 to receive the data word presently in data register 508. In accordance with the above description, each incoming data word is stored in a location defined by the output of **channel counter** 502 in the particular one of the twenty buffer memories defined by the output of the subrate **counter** associated with that **channel**. A more detailed description of the **read-write synchronism** of the buffer memories, e.g., input buffer memory

105, is given in the previously mentioned J. W. Lurtz patent.

Current US Original Classification - CCOR (1):
370/358

Current US Cross Reference Classification - CCXR (1):
370/378